Design of 64 Bit UCSLA for Low Power VLSI Application

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Abstract— This paper presents area and power efficient carry select adder (CSLA). This uses an uniform sized CSLA (UCSLA) with carry skip adder (CSKA) C_{in}=1 instead of using Ripple Carry Adder (RCA) with C_{in}=1. The delay is reduced using CSKA. The achieved area and power of the proposed UCSLA is 1412 μm^2 and 0.0456 mW. The delay is decreased to 47.176 ns.

Index Terms – UCSLA, CSKA, RCA, BEC, Multiplexer, Area, Power, Delay, Verilog-HDL Simulation.

1 INTRODUCTION

ADDITION is basic operation used in many data path logic systems such as adders, multipliers etc. Carry select adder is used for high speed operation by reducing the carry propagation delay. Carry select adders generates many carries and partial sum. The final carry out is selected by the set of multiplexers [1].

The proposed method is to use carry skip adder (CSKA) instead of one ripple carry adder (RCA) with C_{in}=0 in the variable sized CSLA structure to make uniform sized CSLA to consume lower area, power and high speed.

Adders are widely used in all electronic applications for example digital signal processing, microprocessors, and microcontrollers. The key process of the VSLI designer was to reduce the area, power and delay [2].

Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. Ripple carry adders are the slowest even though they are compact in design. Whereas carry look-ahead is the fastest one but consumes more area [3].

The CSLA uses multiple pairs of RCA to generate partial sum and carry by considering carry input C_{in}=0 and C_{in}=1, then the final sum and carry are selected by the multiplexers. It is consider to be area inefficient [4]. The digital adders suffer with the problem of carry propagation delay and also power dissipation is one of the most important design objectives in integrated circuits, after speed [5]. The multiplexer is used to obtain expected output according to the logic state of carry-in signal. The carry select adder achieves low power and area efficiency with an increase in delay [6].

Modified CSLA shows reduction in area and power consumption in comparison with conventional CSLA with a higher delay. The result shows that the Proposed CSLA is better than modified CSLA (MCSLA) [7].

Two types of carry select adder (CSLA) are used to reduce the area and power. One is variable sized carry select adder (VCSLA) and the other is uniform sized carry select adder (UCSLA). The variable sized carry select adder (VCSLA) is used to increase the BEC, so the number of gates is increased [8, 9].

The concept of uniform sized carry select adder (UCSLA) is used to reduce the area, power and delay. In this paper, we proposed the UCSLA with 64 bit inputs.

2 VARIABLE SIZED CARRY SELECT ADDER (VCSLA)

A 64 bit VCSLA is developed. In this VCSLA, RCA is used in upper adder and BEC circuit is used in lower adder part. The VCSLA is used to increase the BEC, so the number of gates is increased.

The 64 bit VCSLA architecture is shown in Fig. 1. It has eleven groups of different size CSLA. The delay and area evaluation of each group are shown in Fig. 2.

The group 1 has only one set of 2 bit RCA with carry-in signal. The carry-out of the RCA is used as control signal in multiplexer.

The group 2 has one set of 2 bit RCA with C_{in}=0 and one set of 3 bit BEC instead of 2 bit RCA with C_{in}=1. The 2 bit RCA with C_{in}=0 is the upper adder and 3 bit BEC is lower adder. The 2 bit input of a and b is given to the upper adder. The output of the upper adder is given to 3 bit BEC circuit and multiplexer. The multiplexer is used to select the output either upper adder or lower adder according to the control signal C_{in} (C_1). Now the sum S_2 and carry-out C_3 is obtained.

Similarly, the other groups are evaluated from the above explanation.

The area and delay of VCSLA is tabulated in Table 1.

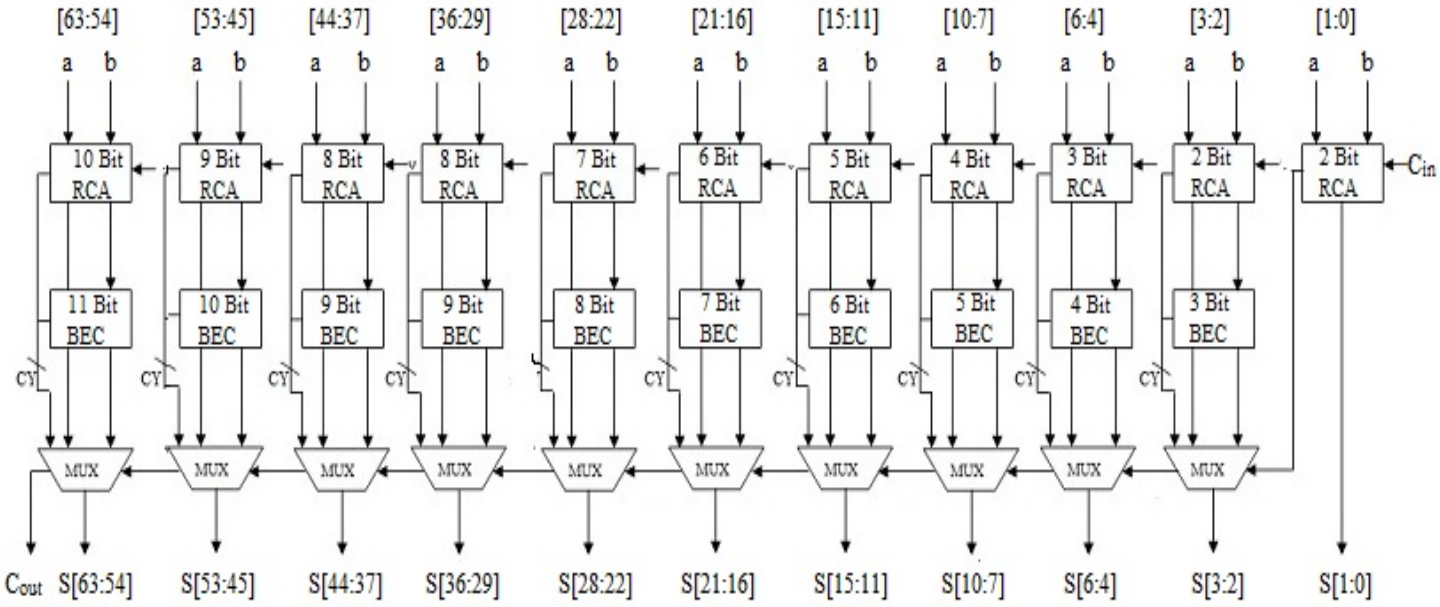


Fig. 1 Sixty Four Bit Regular CSLA Architecture

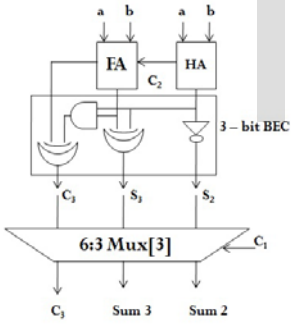


Fig. 2 (a) Group 2 Architecture

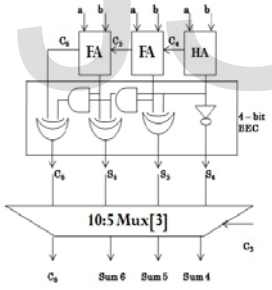
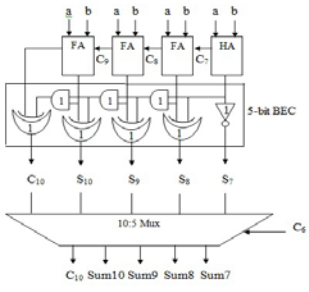


Fig. 2 (b) Group 3 Architecture

TABLE 1
AREA COUNT OF VCSLA

Word Size	*Area (in μm²)*
8 Bit	179
16 Bit	399
32 Bit	839
64 Bit	1552



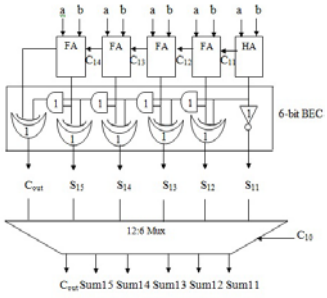


Fig. 2 (c) Group 3 Architecture Fig. 2 (d) Group 4 Architecture

Fig. 2 Delay and area evaluation of VCSLA: (a) group2, (b) group3, (c) group4 and (d) group5. FA is a Full Adder.

3 UNIFORM SIZED CARRY SELECT ADDER (UCSLA)

In his UCSLA, carry skip adder (CSKA) is used for reducing del ay and area compared with VCSLA. The upper adder has the CSKA with C_{in}=0 and the BEC circuit is in the lower ad er instead of RCA with C_{in}=1 in the UCSLA. The 64 bit UC SLA architecture is shown in Fig. 3. The group1 and 2 ar itecture of UCSLA are shown in Fig. 4 and Fig. 5. The CS CA is used to reduce the delay compared with RCA.

The group 1 has only one set of 4 bit CSKA with carry-in sig al. The carry-out of the CSKA is used as control signal in m ltiplexer.

The group 2 has one set of 4 bit CSKA with C_{in}=0 and

one set of 5 bit BEC instead of 4 bit CSKA with C_{in}=1.

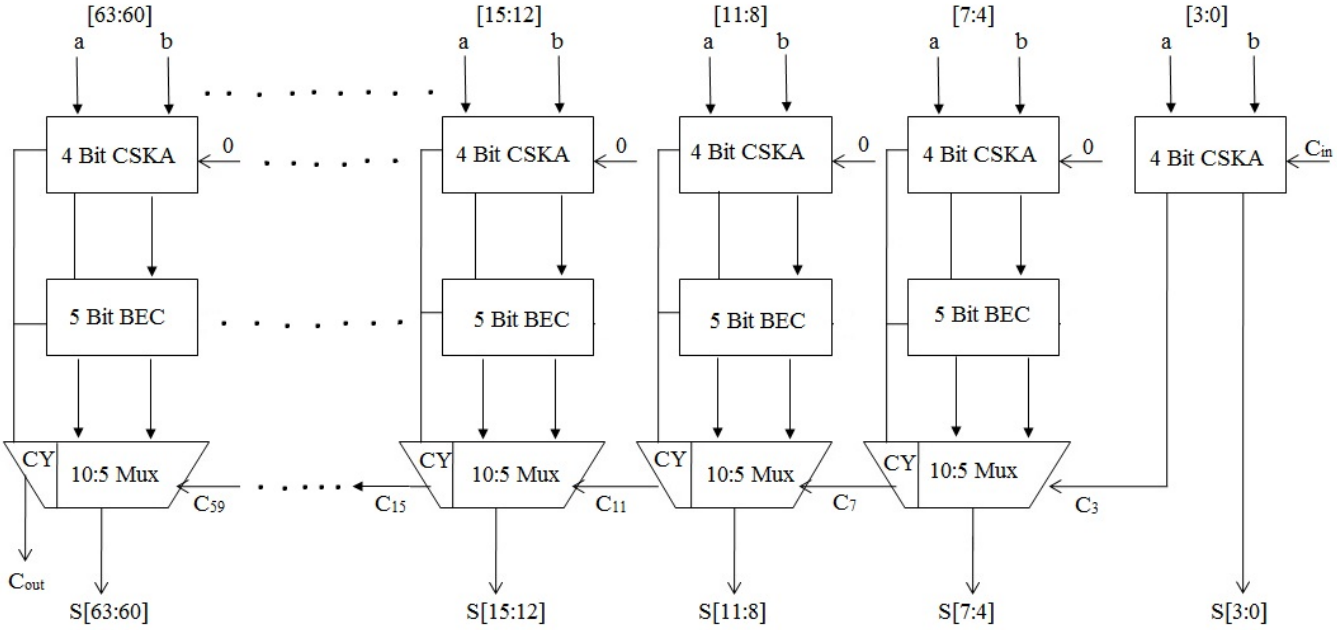


Fig. 3 Sixty Four Bit UCSLA Architecture

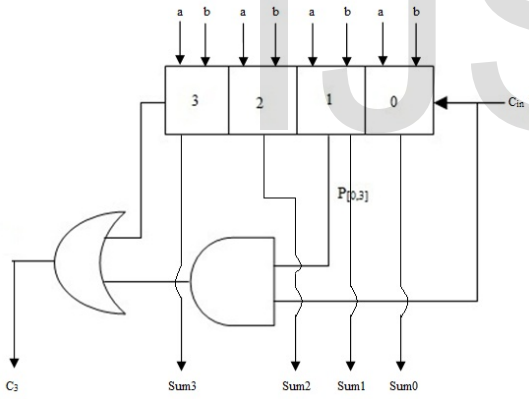


Fig. 4 Four Bit CSKA Architecture

TABLE 2
AREA COUNT OF UCSLA

Word Size	*Area (in μm²)*
8 Bit	162
16 Bit	295
32 Bit	816
64 Bit	1412

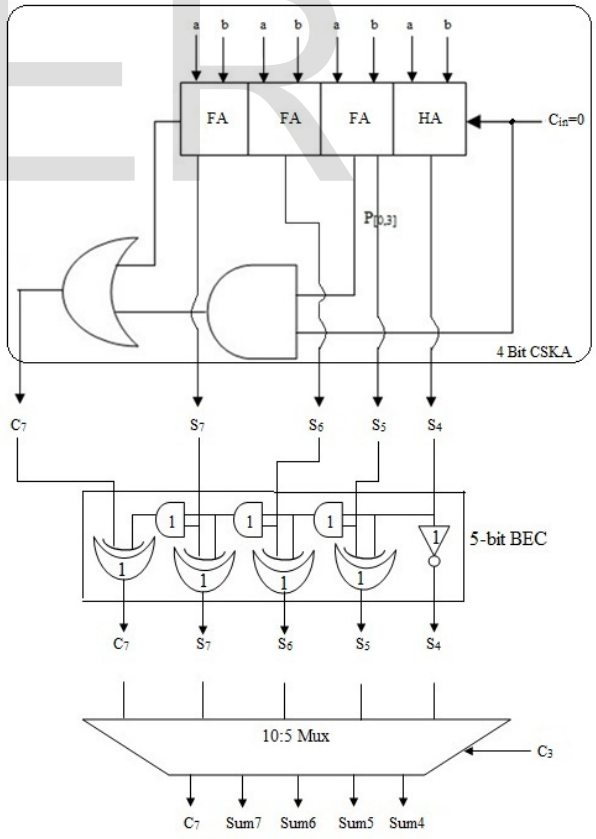


Fig. 5 Group2 UCSLA Architecture

The 4 bit CSKA with C_{in}=0 is the upper adder and 5 bit BEC is

Fig. 5 Simulation Results of CSLA in Modelsim

TABLE 3
COMPARISONS BETWEEN VCLSA AND UCSLA

Word Size	Adder	Area (in μm^2)	Delay (in ns)	Power (in mW)
8-bit	VCSLA	179	30.965	0.0247
	UCSLA	162	28.198	0.0116
16-bit	VCSLA	399	33.158	0.0452
	UCSLA	295	30.008	0.0218
32-bit	VCSLA	839	38.432	0.0691
	UCSLA	816	32.516	0.0386
64-bit	VCSLA	1552	49.218	0.1016
	UCSLA	1412	47.176	0.0456

lower adder. The 4 bit input of a and b is given to the upper adder. The output of the upper adder is given to 5 bit BEC

circuit and multiplexer. The multiplexer is used to select the output either upper adder or lower adder according to the

control signal C_{in} (C_3). Now the sum S_2 and carry-out C_3 is obtained.

$\{C_6, Sum\ [6:4]\}$ = C_3 + Multiplexer
$\{C_{10}, Sum\ [10:7]\}$ = C_6 + Multiplexer
$\{C_{out}, Sum\ [15:11]\}$ = C_{10} + Multiplexer
$\{C_{out}, Sum\ [21:16]\}$ = C_{15} + Multiplexer
$\{C_{out}, Sum\ [31:22]\}$ = C_{21} + Multiplexer

Similarly, the other groups are evaluated from the above explanation. The total number of area counts of UCSLA is tabulated in Table 2.

4 SIMULATION RESULTS AND DISCUSSION

This work has been simulated using Verilog-HDL (Modelsim) in Fig. 5. The adders (of various size 16, 32, 64-bit) are designed and simulated using Modelsim. All the V files (Regular and Modified) are also simulated in Modelsim and corresponding results are compared. After simulation the different size codes are synthesized using Xilinx ISE 9.1i.

The simulated V files are imported into the synthesized tool and corresponding values of delay and area are noted. The synthesized reports contain area and delay values for different sized adders. The similar design flow is followed for both the VCSLA and UCSLA.

Table 3 shows the area and power of the UCSLA significantly reduced by 1412 µm² and 0.0456 mW respectively. The delay also reduced to 47.176 ns. The proposed UCSLA architecture is low power, low area, decreased in delay, simple and efficient.

5 CONCLUSION

In this paper, UCSLA is designed by using single carry skip adder (CSKA) and binary to excess-1 converter (BEC) instead of using one set of ripple carry adder (RCA) with C_{in}=0 to reduce area and power with increase in delay. The compared results show that reducing area and power is 1412 µm² and 0.0456 mW. The reduced delay is 47.176 ns. The UCSLA architecture is low area, low power, simple and efficient for VLSI applications.

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